CLAIMS:

1. Electronic device comprising:

a first chip having an active side and a back side, on which active side the first chip has first and second conductive interconnections;

a second chip having an active side and a back side, on which active side the second chip has first conductive interconnections, the active sides of the first and second chips facing each other, the first conductive interconnections of the chips being mutually connected in electroconductive manner by first metal interconnections;

a substrate having a first side and an opposite second side, which first side faces the active side of the first chip, which substrate comprises a heat sink, conductive interconnections and contact surfaces for external contacting, which heat sink is connected by conductive adhesive with the back of the second chip and which conductive interconnections are electroconductively connected by a second metal interconnection to the second conductive interconnections of the first chip, and which contact surfaces can be contacted on the second side of the substrate; and

an encapsulation of passivating material which envelops the first and second chips and the metal interconnections at any rate substantially and to which the substrate is attached.

2. An electronic device as claimed in claim 1, characterized in that the second metal interconnection has at least partly a lower reflow temperature than the first metal interconnection.

3. An electronic device as claimed in claim 1, characterized in that the substrate accommodates a lead frame which has openings in which the passivating material of the encapsulation is present.

4. An electronic device as claimed in claim 1, characterized in that the second chip in a plane parallel with the active side has a smaller surface area than the first chip.

5. An electronic device as claimed in claim 4, characterized in that the first chip comprises an integrated circuit of essentially passive components while the second chip comprises an integrated circuit of substantially active components.

6. An electronic device as claimed in claim 5, characterized in that the first chip comprises a substrate of doted semiconductor material with pores, which pores extend in a direction in essence perpendicular to the plane parallel with the active side and in which capacitors are defined.

7. An electronic device as claimed in claim 1, characterized in that a third chip having an active side and a back side is present, the active side comprising the third chip of conductive interconnections, the active side of the third chip facing the active side of the first chip, the conductive interconnections of the third chip being mutually electroconductively connected to further conductive interconnections of the first chip by metal wires, the substrate comprising a second heat sink which is connected to the back of the third chip by conductive adhesive.

8. A method of producing an electronic device, comprising the steps of:

providing an ensemble of a first chip and a second chip, each with an active side and a back side, which active sides, comprising first conductive interconnections, are facing each other and the first conductive interconnections are mutually electroconductively connected by a first metal interconnection, the active side of the first chip comprising second conductive interconnections;

providing a substrate having a first and an opposite second side, the substrate comprising a heat sink, conductive interconnections and contact surfaces for external contacting,

applying the ensemble of the first and second chips on the first side of the substrate, while the conductive interconnections having a second metal interconnection are electroconductively connected with the second conductive interconnections of the first chip and the heat sink is connected to the back of the second chip by means of conductive adhesive;

curing of the adhesive;

the re-melting of at least part of the second metal interconnection under relaxation of stress caused by the shrinking of the adhesive layer during curing, and

applying an encapsulation of passivating material around the first and second chips and around the metal interconnections, which material is bonded to the substrate.

9. A method as claimed in claim 8, characterized in that the conductive interconnections in the substrate are located on an elastic layer so that the conductive interconnections can bend to a certain extent and reversibly when the ensemble is mounted on the substrate.

10. A method as claimed in claim 8, characterized in that the second metal interconnection comprises a solder having a reflow temperature that is lower then the reflow temperature of the first metal interconnection.

11. A use of the device as claimed in claim 5, in which the heat sinks are fastened by electroconductive adhesive, during the use of which the – first – heat sink is put to a different voltage than the second heat sink.